PATENT
Docket No.: ACT-317

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit: 2117 Examiner: John J. Tabone Jr.

Serial No.: 10/066,539 Filed: January 30, 2002

In re Application of: Lien et al.

For: TILEABLE FIELD-PROGRAMMABLE GATE ARRAY ARCHITECTURE

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Final Office Action dated July 10, 2007, kindly amend the above-identified application as follows.

In the claims:

1-5. (Canceled)

6. (New) A method for testing the routing circuitry in a field programmable gate array (FPGA) having a first FPGA tile, the routing circuitry having a plurality of first sets of tracks running in a first direction, each set of first tracks having a plurality of individual track segments that are programmably connectable to one another between a first end and a second end by individual programmable elements, the method comprising:

providing a global control signal to simultaneously turn on all of the programmable elements in at least two of the first sets of tracks;

defining individual test inputs to apply to the first end of each of the at least two of the first sets of tracks;

determining an expected logic result for a selected logical combination of the individual test inputs to the at least two of the first sets of tracks;

applying the individual test inputs to the first end of each of the at least two of the first sets of tracks;

performing the selected logical combination on the second ends of the at least two of the first sets of tracks to generate an actual logic result; and

flagging an error if the actual result is not identical with the expected logic result.

7. (New) The method of claim 6 wherein the at least two of the first sets of tracks are a pair of adjacent first sets of tracks.

8. (New) The method of claim 7 wherein the individual test inputs applied to the first ends of the pair of adjacent first sets of tracks are opposite logic states.

9. (New) The method of claim 6 wherein the at least two of the first sets of tracks are a plurality of pairs of adjacent first sets of tracks.

10. (New) The method of claim 9 wherein the individual test inputs applied to the first ends of the plurality of pairs of adjacent first sets of tracks are alternating logic states.

11. (New) The method of claim 10 wherein:

the second ends of odd ones of the plurality of pairs of adjacent first sets of tracks are coupled to inputs of a first wired-NOR circuit having an output and to inputs of a first wired-NAND circuit having an output; and

the second ends of even ones of the plurality of pairs of adjacent first sets of tracks are coupled to inputs of a second wired-NOR circuit having an output and to inputs of a second wired-NAND circuit having an output.

12. (New) The method of claim 6 wherein the first direction is a vertical direction.

13. (New) The method of claim 6 wherein the the routing circuitry also has a plurality of second sets of tracks running in a second direction orthogonal to the first direction, each second set of tracks having a plurality of individual track segments that

are programmably connectable to one another between a first end and a second end by individual programmable elements, the method further comprising:

providing a global control signal to simultaneously turn on all of the programmable elements in at least two of the second sets of tracks;

defining individual test inputs to apply to the first end of each of the at least two of the second sets of tracks;

determining an expected logic result for a selected logical combination of the individual test inputs to the at least two of the second set of tracks;

applying the individual test inputs to the first end of each of the at least two of the second sets of tracks;

performing the selected logical combination on the second ends of the at least two of the second sets of tracks to generate an actual logic result from the at least two of the second sets of tracks; and

flagging an error if the actual result from the at least two of the second sets of tracks is not identical with the expected logic result.

14. (New) The method of claim 13 wherein the at least two of the second sets of tracks are a pair of adjacent second sets of tracks.

15. (New) The method of claim 14 wherein the individual test inputs applied to the first ends of the pair of adjacent second sets of tracks are opposite logic states.

16. (New) The method of claim 13 wherein the at least two of the second sets of tracks are a plurality of pairs of adjacent second sets of tracks.

17. (New) The method of claim 16 wherein the individual test inputs applied to the first ends of the plurality of pairs of adjacent second sets of tracks are alternating logic states.

18. (New) The method of claim 10 wherein:

the second ends of odd ones of the plurality of pairs of adjacent second sets of tracks are coupled to inputs of a third wired-NOR circuit having an output and to inputs of a third wired-NAND circuit having an output; and

the second ends of even ones of the plurality of pairs of adjacent second sets of tracks are coupled to inputs of a fourth wired-NOR circuit having an output and to inputs of a fourth wired-NAND circuit having an output.

REMARKS

Claims 1-5 are presently pending in the above-identified patent application. No claim is allowed. Claims 1-5 have been canceled. Claims 6-18 are newly presented.

Claims 1-3 were rejected pursuant to 35 U.S.C. §103(a) as being unpatentable over Abramovici et al. (US 6,108,806), in view of Andrews et al. (US 6,064,225), and further in view of Kean (US 6,292,018). While these rejections are moot in view of the newly-presented claims, the following remarks are believed to be pertinent to the newly-presented claims.

In item 4 of the Office Action, the examiner characterizes the teachings of Abramovici et al. For the purposes of this argument, the examiner's characterization of Abramovici et al. is assumed to be correct. Inherent in the examiner's characterization of Abramovici et al. is the fact that the reference is directed to testing of the logic blocks 22. Importantly, Abramovici et al. state that "providing a new hybrid method that utilizes only a very limited amount of global routing to provide complete diagnostic testing of an FPGA . . ." is one of the stated aims of the invention disclosed in the reference. Abramovici et al. are testing functional logic.

The entire Abramovici et al. disclosure must assume that the routing resources are completely functional or else the disclosed testing methods would not work. This is a teaching directly in conflict with the present invention, which employs only routing tracks in testing, since only routing tracks are being tested.

In complete contrast with the stated aims of Abramovici et al., the instant invention as presently claimed is directed to testing the routing resources of the FPGA, not the functioning of the logic blocks. The examiner admits that Abramovici et al. do not teach providing a global control signal which turns on all interconnect elements simultaneously. The examiner then states that Abramovici et al. do teach that the FPGA is configured by loading configuration data from a test controller to establish a plurality of blocks under test. However, the examiner incorrectly identifies configuration data as a "global control signal."

Further, the examiner relies on Kean, which he asserts is analogous art, for the teaching of providing a global control signal that turns on all interconnect elements simultaneously. The examiner points to col. 43, lines 52-66, col. 29, lines 31-40, col. 7, lines 39-43, col. 25, line 63 to col. 26, line 25 and col. 28, lines 19-49 as allegedly providing support for this assertion concerning the disclosure of Kean.

It is respectfully asserted that none of these passages from Kean cited by the examiner provides support for the examiner's assertion, which, if correct, would cause the device of Kean to completely fail and become inoperative. The examiner several times mistakenly asserts that Kean discloses "a global control signal which turns on all interconnect elements simultaneously. Kean discloses no such thing, but rather discloses simultaneously writing to multiple locations in configuration memory. If all of the interconnect elements in the Kean FPGA were turned on simultaneously as suggested by the examiner, the device would become one large short circuit and would completely fail to operate. The claims at issue recite turning on all switches in a set of routing tracks to connect the routing tracks from end to end so that continuity can be tested. This is

not the same as turning on all interconnect elements in an FPGA as asserted by the examiner.

With respect to the portions of Kean cited by the examiner, they will be dealt with individually. First, the passage at col. 43, lines 52-66 merely relates to recited advantages of the disclosed system, and neither teaches nor suggests, nor has anything whatsoever to do with providing a global control signal that simultaneously turns on all interconnect elements associated with a set of routing tracks that has a first end and a second end in order to test the continuity of the set of routing tracks, a concept which is neither mentioned nor even hinted at in the cited passage.

Next, the passage at col. 29, lines 31-40 discusses benefits of the wildcard address register, and specifically discusses making identical changes to corresponding cells in different bit slices. The word "simultaneously" is used to indicate that corresponding cells in different bit slices may be changed simultaneously and has nothing to do with simultaneously turning on switches to connect all routing tracks in a set of routing tracks to test the integrity of the tracks in the set. This operation of the wildcard address register neither teaches nor suggests, nor has anything whatsoever to do with providing a global control signal that simultaneously turns on all interconnect elements associated with a set of routing tracks that has a first end and a second end in order to test the continuity of the set of routing tracks, a concept which is neither mentioned nor even hinted at in the cited passage.

Next, the passage at col. 7, lines 39-43 discusses features of the writable control store in the disclosed FPGA. The word "simultaneously" is used to indicate that more than one

word of the control store may be written at the same time and has nothing to do with simultaneously turning on switches to connect all routing tracks in a set of routing tracks to test the integrity of the tracks in the set. As with the previous passages relied upon by the examiner, this operation of the writable control store neither teaches nor suggests, nor has anything whatsoever to do with providing a global control signal that simultaneously turns on all interconnect elements associated with a set of routing tracks that has a first end and a second end in order to test the continuity of the set of routing tracks, a concept which is neither mentioned nor even hinted at in the cited passage.

Next, the passage at col. 25, line 63 to col. 26, line 25 relates to the fact that because FPGA configurations are highly regular, programming time can be saved by writing identical portions of the of the configurations at the same time. The word "simultaneously" is used to indicate that identical blocks of configuration data may be written at the same time to reduce the number of write operations. Again, this concept has nothing to do with simultaneously turning on switches to connect all routing tracks in a set of routing tracks to test the integrity of the tracks in the set. As with the previous passages relied upon by the examiner, this operation of the writable control store neither teaches nor suggests, nor has anything whatsoever to do with providing a global control signal that simultaneously turns on all interconnect elements associated with a set of routing tracks that has a first end and a second end in order to test the continuity of the routing tracks, a concept which is neither mentioned nor even hinted at in the cited passage.

Finally, the passage at col. 28, lines 19-49 again deals with the wildcard register, specifically with writing data to memory cells. The word "simultaneously" is used to

indicate that allows many cell configuration memories in a column of logic blocks to allow regular patterns to be loaded more efficiently. Again, this concept has nothing to do with simultaneously turning on switches to connect all routing tracks in a set of routing tracks to test the integrity of the tracks in the set. As with the previous passages relied upon by the examiner, this operation of the writable control store neither teaches nor suggests, nor has anything whatsoever to do with providing a global control signal that simultaneously turns on all interconnect elements associated with a set of routing tracks that has a first end and a second end in order to test the continuity of the routing tracks in the set, a concept which is neither mentioned nor even hinted at in the cited passage.

In sum, the use of the word "simultaneously" in all of the passages cited by the examiner relate to methods for achieving efficient programming of bit patterns into FPGA configuration memory in contexts that do not disclose or suggest anything about testing the integrity of sets of wiring tracks in an FPGA.

The testing provided for in the rejected claims does not involve testing logic blocks as in Abramovici et al., but only involves testing sets of routing tracks.

With respect to claims 4 and 5, testing of vertical and horizontal routing tracks is specifically recited. The examiner completely fails to deal with the absence of any disclosure in any of the references dealing with these features of the invention.

The simultaneous activation of the switches in the present invention is performed to make a complete circuit from one end of a set of routing tracks to another end of the set

of routing tracks for the purpose of testing the continuity of the set of routing tracks. The examiner's supposed motivation to combine Abramovici et al. and Kean not only misses the mark, but is misapplied to the claims.

In any event, it is respectfully submitted that the newly-presented claims are patentably distinct from the prior art of record. Favorable consideration of this Amendment is respectfully requested.

Applicants believe that the above-identified application is now in condition for allowance and such action is respectfully requested.

If the Examiner has any questions regarding this application or this response, the Examiner is requested to telephone the undersigned at 775-586-9500.

Respectfully submitted,
SIERRA PATENT GROUP, LTD.

Dated: January 8, 2008

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